



Form PTOL-1449 Modified	Docket No. . N1280-00050(TSMC2003-804)	Serial No. 10/804,708
List of Patent and Publications Cited by Applicant (Use several sheets if necessary) U.S. Department of Commerce Patent and Trademark Office	Applicant Chung-Hui Chen	
	Filing Date 03/19/2004	Group Unknown 2838

U. S. PATENT DOCUMENTS

Examiner Initial	Cite No.	Document No.	Kind Code (if known)	Name	Date	Class	Subclass
JH	1.	6,507,087 B1		Yu	01/14/2003	257 829	529
	2.	6,445,606 B1		Khoury	09/03/2002	365 806	96
	3.	6,436,738 B1		Yu	08/20/2002	438 832	132
	4.	6,208,549 B1		Rao et al.	03/27/2001	365 806	96

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Examiner Initial	Cite No.	Country Number Code	Kind Code	Publication Date	Name of Patentee or Applicant	Page, Columns, Lines where Relevant Passages Appeal	T

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initial	Cite No.	(Include name of author in CAPITAL LETTERS, Title of the Article (when appropriate) title of the item (book, magazine, journal, symposium, catalog, etc.) date, pages, volume, issue number(s), publisher, city and/or country where published)	T
JH	5.	Ker, Ming-Dou et al., "CAPACITOR-COUPLE ESD PROTECTION CIRCUIT FOR DEEP-SUBMICRON LOW-VOLTAGE CMOS ASIC", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 4, No. 3, (SEPT. 1996), pp. 307-321	
	6.	Ker, Ming-Dou et al., "COMPLEMENTARY-SCR ESD PROTECTION CIRCUIT WITH INTERDIGITATED FINGER-TYPE LAYOUT FOR INPUT PADS OF SUBMICRON CMOS IC'S", IEEE Transactions on Electron Devices, Vol. 42, No. 7, (JUL 1995), pp. 1297-1304	
	7.	Wu et al., A NEW ON-CHIP ESD PROTECTION CIRCUIT WITH DUAL PARASITIC SCR STRUCTURES FOR CMOS VLSI, IEEE Journal of Solid-State Circuits, Vol. 27, No. 3, (MAR 1992), pp. 274-280	

EXAMINER Sterrett	DATE CONSIDERED 2/23/06
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.